REMARKS/ARGUMENTS

1. In the above referenced Office Action, the Examiner rejected claims 1-3, and 11 under 35 USC § 102 (b) as being anticipated by Hong (U.S. Patent No. 6,147,551); and claims 4-10 and 12-14 under 35 USC § 103 (a) as being unpatentable over Hong (U.S. Patent No. 6,147,551) in view of Soenen (U.S. Patent No. 6,031,480). In addition, the Examiner rejected claims 4, 5, 8-11, and 12-13 under 35 USC § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which the applicant regards as the invention. Further, the Examiner objected to the drawings. These rejections and objections have been traversed and, as such, the applicant respectfully requests reconsideration of the allowability of claims 1 - 14.

2. The drawings have been objected. In particular, the Examiner stated that the prior art of Figure 1 is not labeled as such. The applicant respectfully disagrees.

The specification of the present patent application is clear that Figure 1 depicts an embodiment of the present invention. Please see page 2, Brief Description of the Drawings, wherein Figure 1 is referenced as illustrating an analog front-end in accordance with the present invention. Further, on page 3, lines 10 and 11, the specification includes "the present invention can be more fully described with reference to Figures 1 through 4." Thus, Figure 1 is not a prior art figure and no correction is needed.

3. Claims 4, 5, 8-11, and 12-13 have been rejected under 35 USC § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which the applicant regards as the invention. In particular, the Examiner stated that claims 4, 5, 8, 9, 12, and 13 are unclear as to what is meant by divider. The Examiner questions as to whether it is a voltage divider. The Examiner further stated that in claim 4 the limitation of "a divider operably coupled to the input" is confusing; in claim 10, the term "hybrid circuit" is too broad; and in claim 11, the limitation of a "second feedback capacitor" is confusing without a first feedback capacitor.

a. In claims 4, 5, 8, 9, 12, and 13 it is unclear as to what is meant by divider. The applicant respectfully disagrees. As is presently claimed, the divider includes a tap that provides a common mode voltage of the input signal or of the power supply. Thus, a divider is functionally described to produce a common mode voltage of the input signal or of the power supply at a tap of the divider. The applicant believes that such a functional description provides sufficient description to one of average skill in the art, especially in light of the teachings of the specification, and the present rejection should be withdrawn.

b. The Examiner further stated that in claim 4 the limitation of "a divider operably coupled to the input" is confusing. Claims 4, 8, and 12 have been amended to clarify that the divider is operably coupled to the input signal.

c. In claim 10, the term "hybrid circuit" is too broad. The applicant respectfully disagrees. The term is clearly supported by the specification and in the Figures. In particular, Figure 1 illustrates a hybrid circuit 16 and the correspond text on page 3, line 19 through page 4, line 13 describes the hybrid circuit 16. As such, the applicant believes that the present rejection should be withdrawn.

d. In claim 11, the limitation of a "second feedback capacitor" is confusing without a first feedback capacitor. The applicant respectfully disagrees. With reference to claim 11, the element following the second feedback capacitor is a first feedback capacitor. As such, the applicant believes that this rejection should be withdrawn.

4. Claims 1-3, and 11 have been rejected under 35 USC § 102 (b) as being anticipated by Hong (U.S. Patent No. 6,147,551). In particular, the Examiner stated that Hong teaches in Figure 5 a switched-capacitor circuit comprising a first capacitor (222), a first voltage reference module (218), second voltage reference module (215), a first switch (233) operable to couple an input signal to a first plate of the first capacitor, a second switch (221) to couple a first plate of the first capacitor to the second reference voltage module (215), a third switch (232) operable to couple a second plate of the first voltage reference, a fourth switch (223) operable to provide a charge transfer from the second plate of the first capacitor (222) and an operational amplifier (262) that includes a first input, second input, and a differential output, wherein the first input is operably coupled to the

fourth switching element and the second input is operably coupled to the second reference voltage (215), a first feedback capacitor (263) coupled to the first input and the differential output of the operational amplifier, a second feedback capacitor (262) coupled to the second input and the differential output of the operational amplifier. The above-mentioned components can all be incorporated into a delta-sigma modulator. The applicant respectfully disagrees.

As is claimed in claims 1 and 11, during the first interval, the first plate of the capacitor is coupled to the input signal and the second plate is coupled to the first reference voltage. During the second interval, the first plate is coupled to the second reference voltage and the second plate is coupled to transfer the charge.

In contrast, as shown in figure 5 of Hong, during a first interval (Φ1), capacitor 222 is coupled to VREF 215 and to VREF1 215 via switches 231 and 232. During a second interval (Φ2), the capacitor is coupled to VREF 215 and to capacitor 224 via switches 221 and 223. Clearly the switching of claims 1 and 11 is not anticipated by Hong as the Examiner has referenced.

Claims 2 and 3 are dependent upon claim 1, which has been shown to overcome the present rejection. Since each of claims 2 and 3 introduce additional patentable subject matter, the applicant believes that claims 2 and 3 overcome the present rejection.

5. Claims 4-10 and 12-14 have been rejected under 35 USC § 103 (a) as being unpatentable over Hong (U.S. Patent No. 6,147,551) in view of Soenen (U.S. Patent No. 6,031,480). In particular, the Examiner stated that Hong discloses the essential features of the claimed invention as forth above except for the voltage divider circuit coupled to an input signal and a power supply, a comparator to compare the input signal with a reference, a decimation filter, a digital to analog converter to produce a transmit signal and an analog to digital convert and a second operational amplifier. However, Soenen teaches in Figure 3 an analog to digital convert apparatus and method that has a voltage divider circuit coupled to an input signal (20) and a power supply (42), operational amplifiers (32) and (34) to compare an input signal with a reference signal, and in Figure 2, a digital to analog converter (26) to produce a transmit signal, and an analog to digital converter (24). Therefore, it would have been obvious to one of ordinary skill in the art to incorporate these design techniques of Soenen into the system of Hong to improve system performance and reliability. It would have been further obvious to include a decimation filter in the circuit to reduce the final output code frequency and make the computations more manageable and to have some interface or hybrid circuit to receive and/or transmit a signal. The applicant respectfully disagrees.

As presented above, Hong does not anticipate the present claimed invention as stated by the Examiner. Further, the resistive divider (40, 44, and 46) of Soenen does not couple to the input (20), but couples to a

positive voltage rail 42 and to ground. Its taps produces comparative voltages for the flash ADC 24.

As taught by Soenen, the ADC 24 is a flash converter, which, as known in the art, is a completely different architecture than a sigma-delta ADC, as is presently claimed. The flash ADC 24 of Soenen includes a resistive divider, comparators 32 and 34, and a decode logic 52 to produce a digital output from an analog input. It does not include a sigma-delta modulator or a decimation filter, since it is an entirely different ADC architecture. As such, the flash ADC 24 has no need for switched capacitors, thus combining the teaching of Hong's switch capacitors is an improper combination and does not render the present claims obvious.

For the foregoing reasons, the applicant believes that claims 1 - 14 are in condition for allowance and respectfully request that they be passed to allowance.

The Examiner is invited to contact the undersigned by telephone or facsimile if the Examiner believes that such a communication would advance the prosecution of the present invention.

RESPECTFULLY SUBMITTED,

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